

## ABSTRACT OF THE DISCLOSURE

5            A wireless communications architecture having first and second  
synchronous memory devices coupled to a virtual channel memory controller by  
corresponding first and second data buses, and a shared address and control bus  
interconnecting the virtual channel memory controller and the first and second  
synchronous memory devices. The first and second synchronous memory devices  
are addressed with the shared address bus, and the first and second memory  
locations are accessed via the first and second data buses, respectively.